I. COMMUNICATIONS TECHNICAL SUPPLEMENT

This section contains information intended for advanced users planning to do custom programming with the QS-100D. The information presented here is a technical description of the interface to the 16450, 16550, or 16570 UART.

The 16450 UART is an improved functional equivalent of the 8250 UART, performing serial-to-parallel conversion on received data and parallel-to-serial conversion on output data. Designed to be compatible with the 16450, the 16550 and 16750 UARTs enter character (non-FIFO) mode on reset. In this mode, the 16550 and 16750 appear as a 16450 to application software.

An additional mode, FIFO mode, can be invoked through software to reduce CPU overhead. FIFO mode increases performance by providing two hardware buffers, one for transmit and one for receive. The 16550 has 16 byte buffers while the 16750's are 64 bytes. Operating in FIFO mode can reduce the frequency of interrupts issued to the CPU by the UART.

Other features of the 16450, 16550, and 16750 include:

- Programmable baud rate, character length, parity, and number of stop bits.
- Automatic control of start, stop, and parity bits.
- Independent and prioritized interrupts.
- Transmit clock output / receive clock input.
- CTS and RTS Auto-flow control (16750 only)

The QS-100D's serial ports are controlled by four 16450, 16550, or 16750 UARTs. The serial ports will generate interrupts in accordance with the bits set in the interrupt enable register of the UARTs. In order to maintain compatibility with earlier personal computer systems, the user-defined output OUT2 is used as an external interrupt enable and must be set active for interrupts to be generated. OUT2 is accessed through the UART's MODEM control register.

The following pages provide a brief summary of the internal registers available within the 16450, 16550, and 16750 UARTs. Registers and functions specific to the 16550 and 16750 will be indicated with **boldface** notations. Registers and functions specific to the 16750 only will be indicated with ***boldface italic*** notations.

Accessing The Serial Port Registers

Figure 14 lists the address map for the 16450, 16550, and 16750 UARTs. Each register can be accessed by reading from or writing to the proper I/O address. This I/O address is determined by adding an offset to the base address set for the particular serial port. The base address is set using DIP switches on the QS-100D (see section III).

Notice that two locations access different registers depending on whether an I/O read or I/O write is attempted. Address [base+0] accesses the receive buffer on an I/O read, or the transmit buffer on an I/O write. Address [base+2] accesses the Interrupt Identification register on an I/O read or the FIFO control register **(16550 and 16750 only)** on an I/O write. Also, notice that if address [base+0] or [base+1] is used with the DLAB bit from the Line Control Register set to '1', the baud rate divisor latches are accessed.

NOTE: All figures displaying bitmapped registers are formatted such that bit 7 is the high-order bit.

UART Addressing		Register Description
DLAB	I/O Address	
0	Base + 0	Receive buffer (read) Transmit holding register (write)
0	Base + 1	Interrupt enable
X	Base + 2	Interrupt identification (read) FIFO control (write) **(16550 and 16750)**
X	Base + 3	Line control
X	Base + 4	MODEM control
X	Base + 5	Line status
X	Base + 6	MODEM status
X	Base + 7	Scratchpad
1	Base + 0	Baud rate divisor latch (LSB) *
1	Base + 1	Baud rate divisor latch (MSB) *
(X = don't care) * DLAB in Line Control Register must be set to access baud rate divisor latch.		

Figure 1 --- Serial port register address map for 16450/16550/16750 UART

Interrupt Enable Register

This register is located at I/O address [base+1]. It enables the five types of UART interrupts. Interrupts can be totally disabled by setting all of the enable bits in this register to a logic 0. Setting any bit to a logic 1 enables that particular interrupt.

BIT	DESCRIPTION
7	0 --- reserved
6	0 --- reserved
5	0 --- reserved
4	0 --- reserved
3	**EDSSI** --- MODEM Status Interrupt: When set (logic 1), enables interrupt on clear to send, data set ready, ring indicator, and data carrier detect.
2	**ELSI** --- Receiver Line Status Interrupt: When set (logic 1), enables interrupt on overrun, parity, framing errors, and break indication.
1	**ETBEI** --- Transmitter Holding Register Empty Interrupt: When set (logic 1), enables interrupt on transmitter holding register empty.
0	**ERBI** --- Received Data Available Interrupt: When set (logic 1), enables interrupt on received data available. For **16550 and 16750 FIFO mode**, interrupts are also enabled for receive FIFO trigger level reached and for receive timeout.

Figure 2 --- Interrupt Enable Register bit definitions

Interrupt Identification Register

This read-only register is located at I/O address [base+2]. When this register is read, the UART freezes all interrupts and indicates the highest priority interrupt. During this time, new interrupts are detected by the UART, but are not reported in this register until the access completes.

For the **16550 and 16750**, this register can be used to indicate whether the FIFO mode is engaged by examining bits 6 and 7. For the ***16750 only*** bit 5 can be used to indicate whether the 64 byte FIFO has been enabled.

BIT	DESCRIPTION
7	**FFE** --- FIFO enable: **(16550 and 16750)** When logic 1, indicates FIFO mode enabled. Always logic 0 for the 16450.
6	**FFE** --- FIFO enable: **(16550 and 16750)** When logic 1, indicates FIFO mode enabled. Always logic 0 for the 16450.
5	**64FFE** --- 64 byte FIFO enabled ***(16750 only)*** When logic 1, indicates 64 byte FIFO enabled. Always logic 0 for the 16450 / 16550.
4	0 --- reserved
3 2 1	**IID2** --- **IID1** --- **IID0** --- Interrupt Identification: Indicates highest priority interrupt pending if any. **See Figure 17.** NOTE: IID2 is always a logic 0 on the 16450 or in non-FIFO mode on the 16550.
0	**IP** --- Interrupt pending: When logic 0, indicates that an interrupt is pending and the contents of the interrupt identification register may be used to determine the interrupt source. **See Figure 17.**

Figure 3 --- Interrupt Identification Register bit definitions

Figure 17 gives the detail of the IIDx bits in the Interrupt Identification Register. These bits are examined to determine the source of an interrupt.

IIDx bits			IP	Priority	Interrupt Type
2	1	0			
don't care			1	N / A	**None**
0	1	1	0	1st	**Receiver Line Status:** Indicates overrun, parity, framing errors or break interrupts. The interrupt is cleared by reading the line status register.
0	1	0	0	2nd	**Received Data Ready :** Indicates receive data available. The interrupt is cleared by reading the receive buffer. In **16550 and 16750 FIFO mode**, indicates the receiver FIFO trigger level has been reached. The interrupt is reset when the FIFO drops below the trigger level.
1	1	0	0	2nd	**Character Timeout (16550 and 16750 FIFO mode)**: Indicates no characters have been removed from or input to the receiver FIFO for the last four character times and there is data present in the receiver FIFO. The interrupt is cleared by reading the receiver FIFO.
0	0	1	0	3rd	**Transmitter Holding Register Empty**: Indicates the transmitter holding register is empty. The interrupt is cleared by reading the interrupt identification register or writing to the transmitter holding register. **(Indicates transmit FIFO empty for 16550 and 16750.)**
0	0	0	0	4th	**MODEM Status**: Indicates clear to send, data set ready, ring indicator, or data carrier detect have changed state. The interrupt is cleared by reading the MODEM status register.

Figure 4 --- IIDx bit decoding

Fifo Control Register *(16550 And 16750)*

This register, which applies only to the 16550 and 16750 UARTs, is a write-only register located at I/O address [base+2]. It is used to enable the FIFO mode, clear the FIFOs, set the threshold level for the receive FIFO to generate interrupts, and to set the mode under which the device uses DMA. Note that DMA mode is NOT supported by the QS-100D.

<table>
<tr><th>BIT</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td>7

6</td><td>RXT1 ---

RXT0 ---</td><td>Receiver FIFO Trigger Level (16550 and 16750):
Determines the trigger level for the receiver FIFO interrupt
<table>
<tr><th>RXT1</th><th>RXT0</th><th>Receiver FIFO trigger level (bytes)
16550</th><th>16750</th></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>4</td><td>16</td></tr>
<tr><td>1</td><td>0</td><td>8</td><td>32</td></tr>
<tr><td>1</td><td>1</td><td>14</td><td>56</td></tr>
</table></td></tr>
<tr><td>5</td><td colspan="2">EN64 --- Enable 64 byte FIFO (16750 only)
When set (logic 1) and DLAB is set (logic 1), enables the 16750's 64 byte FIFOs. If logic, the 16750 operates in 16550 mode. This bit is always 0 for the 16450/16550.</td></tr>
<tr><td>4</td><td colspan="2">0 --- reserved</td></tr>
<tr><td>3</td><td colspan="2">DMAM --- DMA mode select (16550 and 16750):
When set (logic 1), RxRDY and TxRDY change from mode 0 to mode 1 for DMA transfers. (DMA mode is not supported on the QS-100D.)</td></tr>
<tr><td>2</td><td colspan="2">XRST --- Transmit FIFO reset (16550 and 16750):
When set (logic 1), all bytes in the transmitter FIFO are cleared and the counter is reset. The shift register is not cleared. XRST is self-clearing.</td></tr>
<tr><td>1</td><td colspan="2">RRST --- Receive FIFO reset (16550 and 16750):
When set (logic 1), all bytes in the receiver FIFO are cleared and the counter is reset. The shift register is not cleared. RRST is self-clearing.</td></tr>
<tr><td>0</td><td colspan="2">FE --- FIFO enable (16550 and 16750):
When set (logic 1), enables transmitter and receiver FIFOs. When cleared (logic 0), all bytes in both FIFOs are cleared. This bit must be set when other bits in the FIFO control register are written to or the bits will be ignored.</td></tr>
</table>

Figure 5 --- 16550 and 16750 FIFO Control Register bit definitions

Line Control Register

This register is located at I/O address [base+3]. It is used for specifying the format of the asynchronous serial data to be processed by the UART, and to set the Divisor Latch Access Bit (DLAB) allowing access to the baud rate divisor latches.

<table>
<tr><th>BIT</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td>7</td><td colspan="2">DLAB --- Divisor latch access bit:
DLAB must be set to logic 1 to access the baud rate divisor latches. DLAB must be set to logic 0 to access the receiver buffer, transmitting holding register and interrupt enable register.</td></tr>
<tr><td>6</td><td colspan="2">BKCN --- Break control:
When set (logic 1), the serial output (SOUT) is forced to the spacing state (logic 0).</td></tr>
<tr><td>5</td><td>STKP --- Stick parity:
Forces parity to logic 1 or logic 0 if parity is enabled.</td><td rowspan="3"><table><tr><th>STKP</th><th>EPS</th><th>PEN</th><th>PARITY</th></tr><tr><td>x</td><td>x</td><td>0</td><td>None</td></tr><tr><td>0</td><td>0</td><td>1</td><td>Odd</td></tr><tr><td>0</td><td>1</td><td>1</td><td>Even</td></tr><tr><td>1</td><td>0</td><td>1</td><td>Logic 1</td></tr><tr><td>1</td><td>1</td><td>1</td><td>Logic 0</td></tr></table></td></tr>
<tr><td>4</td><td>EPS --- Even parity select:
Selects even or odd parity if parity is enabled.</td></tr>
<tr><td>3</td><td>PEN --- Parity enable:
Enables parity on transmission and verification on reception.</td></tr>
<tr><td>2</td><td rowspan="2">STB --- Number of stop bits:
Sets the number of stop bits transmitted.

WLS1 --- Word length select:
Determines the number of bits per
WLS0 --- transmitted word.</td><td rowspan="2"><table><tr><th>STB</th><th>WLS1</th><th>WLS0</th><th>WORD LEN</th><th>STOP BITS</th></tr><tr><td>0</td><td>0</td><td>0</td><td>5 bits</td><td>1</td></tr><tr><td>0</td><td>0</td><td>1</td><td>6 bits</td><td>1</td></tr><tr><td>0</td><td>1</td><td>0</td><td>7 bits</td><td>1</td></tr><tr><td>0</td><td>1</td><td>1</td><td>8 bits</td><td>1</td></tr><tr><td>1</td><td>0</td><td>0</td><td>5 bits</td><td>1.5</td></tr><tr><td>1</td><td>0</td><td>1</td><td>6 bits</td><td>2</td></tr><tr><td>1</td><td>1</td><td>0</td><td>7 bits</td><td>2</td></tr><tr><td>1</td><td>1</td><td>1</td><td>8 bits</td><td>2</td></tr></table></td></tr>
<tr><td>1

0</td></tr>
</table>

Figure 6 --- Line Control Register bit definitions

Modem Control Register

This register is located at I/O address [base+4], and is used to control the interface with the modem or device used in place of a modem. This register allows the states of the "modem control signals" to be changed. These are DTR (Data Terminal Ready) and RTS (Request To Send). It is also possible to place the UART in a loopback mode for testing. Finally, the user-defined outputs OUT1 and OUT2 are controlled from this register.

The QS-100D handles the OUT1 and OUT2 signals in the manner appropriate for maintaining compatibility with standard PC serial ports:

- The OUT1 output is not connected.
- The OUT2 output is used to globally enable interrupts to the computer. It should be active at all times if interrupts are being used.

BIT	DESCRIPTION
7	0 --- reserved
6	0 --- reserved
5	**AFE** --- Auto-flow Control Enable ***(16750 only)***: When set (logic 1), enables the UART's autoflow. RTS AFE Auto-flow configuration X 0 Auto-RTS and Auto-CTS disabled 0 1 Auto-CTS only enabled 1 1 Auto-CTS and Auto RTS enabled
4	**LOOP** --- Loopback enable: When set (logic 1), the transmitter shift register is connected directly to the receiver shift register. The MODEM control inputs are internally connected to the MODEM control outputs and the outputs are forced to the inactive state. All characters transmitted are immediately received to verify transmit and receive data paths. Transmitter and receiver interrupts still operate normally. MODEM control interrupts are available but are now controlled through the MODEM control register.
3	**OUT2** --- Output 2: When this bit is set (logic 1), the OUT2 output is forced active to a logic 0. When cleared (logic 0), the OUT2 output is forced inactive to a logic 1. Used for interrupt enable on the QS-100D.
2	**OUT1** --- Output 1: When this bit is set (logic 1), the OUT1 output is forced active to a logic 0. When cleared (logic 0), the OUT1 output is forced inactive to a logic 1. Not connected on the QS-100D.
1	**RTS** --- Request to send: When this bit is set (logic 1), the RTS output is forced active to a logic 0. When cleared (logic 0), the RTS output is forced inactive to a logic 1.
0	**DTR** --- Data terminal ready: When this bit is set (logic 1), the DTR output is forced active to a logic 0. When cleared (logic 0), the DTR output is forced inactive to a logic 1.

Figure 7 --- Modem Control Register bit definitions

Line Status Register

This register is located at I/O address [base+5]. It is used to provide various types of status information concerning the data transfer. As shown below, the Line Status Register indicates several types of errors, an empty transmit buffer, a ready receive buffer, or a break on the receive line.

BIT	DESCRIPTION
7	**FFRX** --- Error in RCVR FIFO **(16550 and 16750 FIFO mode only)**: Always logic 0 in 16450 or non-FIFO mode in a 16550/16750. Indicates one or more parity errors, framing errors, or break indications in the receiver FIFO. FFRX is reset by reading the line status register.
6	**TEMT** --- Transmitter empty: Indicates the transmitter holding register or FIFO **(16550 and 16750)** AND the transmitter shift register are empty and are ready to receive new data. TEMT is reset by writing a character to the transmitter holding register.
5	**THRE** --- Transmitter holding register empty: Indicates the transmitter holding register or FIFO **(16550 and 16750)** is empty and it is ready to accept new data. THRE is reset by writing data to the transmitter holding register.
4	**BI** --- Break interrupt: Indicates the receive data input has been in the spacing state (logic 0) for longer than one full word transmission time. In **16550 and 16750 FIFO mode**, only one zero character is loaded into the FIFO and transfers are disabled until the serial data input goes to the mark state (logic 1) and a valid start bit is received.
3	**FE** --- Framing error: Indicates the received character had an invalid stop bit. The stop bit following the last data or parity bit was a 0 bit (spacing level).
2	**PE** --- Parity error: Indicates that the received data does not have the correct parity.
1	**OE** --- Overrun error: Indicates the receive buffer was not read before the next character was received and the character is destroyed. In **16550 and 16750 FIFO mode**, indicates the receive FIFO is full and another character has been shifted in. The character in the shift register is destroyed but is not transferred to the FIFO.
0	**DR** --- Data ready: Indicates data is present in the receive buffer or FIFO **(16550 and 16750)**. DR is reset by reading the receive buffer register or receiver FIFO.

Figure 8 --- Line Status Register bit definitions

Bits BI, FE, PE, and OE are the sources of receiver line status interrupts. The bits are reset by reading the line status register. **In 16550 and 16750 FIFO mode**, these bits are associated with a specific character in the FIFO and the exception is revealed only when that character reaches the top of the FIFO.

Modem Status Register

This register is located at I/O address [base+6]. It reports on the status of signals coming from the modem or equipment used in place of a modem. It allows the current states of "modem control signals" to be sensed. These signals include the DCD (Data Carrier Detect), RI (Ring Indicator), DSR (Data Set Ready), and CTS (Clear To Send).

The Modem Status Register also provides change information for each of these signals. When a modem control signal changes state, the appropriate change bit is set to logic 1. The change bits (3, 2, 1, and 0) are reset to logic 0 whenever the Modem Status Register is read.

A modem status interrupt is generated whenever any of bits 3, 2, 1 or 0 is set by the UART to a logic 1.

BIT	DESCRIPTION
7	**DCD** --- Data carrier detect: Complement of the DCD input.
6	**RI** --- Ring indicator: Complement of the RI input.
5	**DSR** --- Data set ready: Complement of the DSR input.
4	**CTS** --- Clear to send: Complement of the CTS input.
3	**DDCD** --- Delta data carrier detect: Indicates the Data Carrier Detect input has changed state. Cleared when this register is read.
2	**TERI** --- Trailing edge ring indicator: Indicates the Ring Indicator input has changed from a low to a high state. Cleared when this register is read.
1	**DDSR** --- Delta data set ready: Indicates the Data Set Ready input has changed state. Cleared when this register is read.
0	**DCTS** --- Delta clear to send: Indicates the Clear to Send input has changed state. Cleared when this register is read.

Figure 9 --- Modem Status Register bit definitions

Scratchpad Register

This register is located at I/O address [base+7]. It is not used by the 16450, 16550, or 16750. It may be used by the programmer for temporary data storage. The Scratchpad Register is eight bits wide and can be read or written.

FIFO Interrupt Mode Operation *(16550 AND 16750 UARTS)*

When The Receiver Fifo And Receiver Interrupts Are Enabled:

1. The receive data interrupt is issued when the receive FIFO reaches the trigger level. The interrupt is cleared as soon as the receive FIFO falls below the trigger level.
2. The Interrupt Identification Register's receive data available indicator is set and cleared along with the receive data interrupt when the receive FIFO falls below the trigger level.
3. The data ready indicator is set as soon as a character is transferred into the receiver FIFO and is cleared when the FIFO is empty.
4. A FIFO timeout interrupt will occur if the receive FIFO contains at least one character, at least four character-times have passed since receipt of the last character, and the last read of the FIFO by the CPU was done more than four character-times ago.
5. Timeout interrupts are cleared when a read of the receive FIFO is done.
6. The receive FIFO timeout timer is reset whenever a new character is received into the FIFO or a read of the FIFO is done.

When The Transmit Fifo And Transmit Interrupts Are Enabled:

1. The transmitter holding register empty interrupt occurs when the transmit FIFO is empty, and is cleared when a character is written to the FIFO or when the Interrupt Identification Register is read.
2. Transmitter FIFO empty indications are delayed by one character-time less the last stop bit time when the transmitter holding register is empty and there have not been at least two bytes together in the transmit FIFO since the last time the transmitter holding register was empty.
3. The first transmitter interrupt after enabling the FIFO mode will be immediate if that interrupt is enabled.

FIFO Polled Mode Operation *(16550 AND 16750 UARTS)*

The receiver and transmitter are operated independently, which would allow either or both to be used in a polled mode rather than using interrupts to determine when the UART needs to be serviced.

To use the UART in a polled mode, the software is responsible for continuously checking for the conditions that normally cause interrupts to occur. This would be done using the Line Status Register.

1. The Data Ready bit will be set to logic 1 whenever there is at least one byte in the receive FIFO.
2. Errors can be detected using the various error bits.
3. The Transmitter Holding Register Empty bit can be used to determine when the transmit FIFO is empty.
4. The Transmitter Empty bit indicates that the transmitter shift register is empty as well as the transmit FIFO being empty.
5. Trigger levels and FIFO timeouts do not apply. Both FIFOs are fully capable of holding multiple characters at any time.

Auto-Flow Control (16750 Only)

The 16750 UART has the ability to control the status of the RTS and CTS lines; this is known as Auto-Flow.

If Auto-RTS mode is enabled, the RTS signal is deasserted when the receiver FIFO reaches its trigger level. Since the sending device may not immediately recognize the deassertion of RTS, it may send one more byte after RTS is deasserted. RTS is reasserted when the receiver FIFO is emptied by reading the receiver buffer register.

When Auto-CTS is enabled, CTS must be active for the transmitter to send its next byte. In this mode, a change in CTS does not result in an interrupt to the host.

Baud Rate Selection

DESIRED BAUD RATE	DIVISOR LATCH VALUE	ERROR BETWEEN DESIRED AND ACTUAL VALUES (%)
50	2304	-
75	1536	-
110	1047	0.026
150	768	-
300	384	-
600	192	-
1200	96	-
1800	64	-
2000	58	0.69
2400	48	-
3600	32	-
4800	24	-
7200	16	-
9600	12	-
19200	6	-
38400	3	-
56000	2	2.86

Figure 10 --- Divisor Latch settings for common baud rates using 1.8432 MHz input clock